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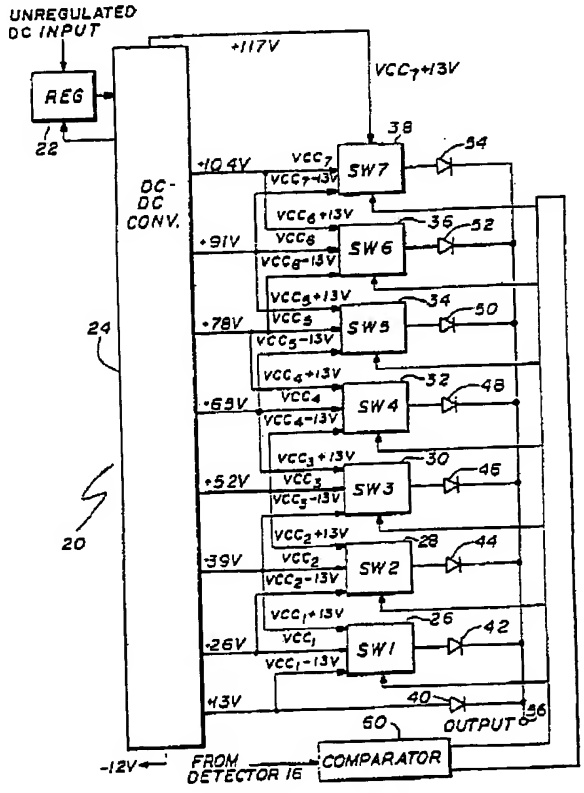
(54) Title: ENVELOPE AMPLIFIER

(57) Abstract

A high efficiency envelope amplifier (20) is disclosed. The invention includes a power supply (24), a comparator (60), and several switches (26-38). The power supply (24) is capable of providing multiple outputs. The comparator (60) measures the amplitude of an input signal against one of several threshold levels. When the input signal is within a predetermined range, a selected power supply output is switched onto the output path. Since the present invention incrementally switches small amounts of power, switching losses are substantially mitigated.



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ENVELOPE AMPLIFIER

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to amplifiers. More specifically, the present invention relates to high frequency RF amplifiers employing an envelope elimination and restoration technique (EER).

While the present invention is described herein with reference to a illustrative embodiment for a particular application, it is understood that the invention is not limited thereto. Those of ordinary skill in the art and access to the teachings provided herein will recognize additional modifications, applications and embodiments within the scope thereof.

2. Description of the Related Art

To improve the efficiency of linear radio frequency (RF) amplifiers certain techniques have been developed. Envelope elimination and restoration (EER) is one such technique. As described in "Single Sideband Transmission by Envelope Elimination and Restoration" by L. R. Kahn in the July 1952 Proceedings of the I.R.E., pp. 803-806 and in "Comparison of Linear Single-Sideband Transmitters with Envelope Elimination and Restoration Single-Sideband Transmitters" by L. R. Kahn, in the December 1956 Proceedings of the I.R.E., pp. 1706-1712, this scheme provides a method for amplifying a variable amplitude signal by separately amplifying its phase and envelope

components. The input signal is amplitude limited so that a signal containing only phase modulation is amplified by the high efficiency RF amplifier. This permits the operation of a high efficiency RF amplifier, e.g. a Class C amplifier, at constant drive power. The envelope of the input signal is processed in a separate path to provide a modulated power supply for the RF amplifier. As the output of the RF amplifier varies in response to its supply, the envelope of the signal is restored as part of the properly amplified output signal.

In a typical system, the modulator includes an envelope detector and an envelope amplifier. If the modulator is of sufficiently high efficiency, the overall efficiency of the EER system may exceed that of the linear Class A or Class B amplifier that would otherwise be required to deal with the variable amplitude signal. The efficiency of the envelope amplifier is therefore a driver with respect to the efficiency of the overall system. Thus, variable duty cycle high switching speed converters have been used as envelope amplifiers. However, the switching speed of variable duty cycle high switching speed converters must be sufficiently higher than the signal bandwidth to permit removal of the switching frequency components by a suitable filter. For wide bandwidth signals, the switching frequency may be so high that the attendant switching losses significantly degrade the amplifier efficiency. This is a significant limitation on the use of variable duty cycle switching converters as envelope amplifiers.

There is therefore a need in the art for an envelope amplifier for use with an EER system which offers high frequency operation with significantly reduced switching losses.

SUMMARY OF THE INVENTION

The problems of conventional envelope elimination and restoration systems are addressed by the envelope amplifier of the present invention which includes a power supply, a comparator and a number of switches. The power supply is capable of providing selectable output voltages. The comparator measures the amplitude of an input signal against one of several threshold levels. When the input signal is in a predetermined range, a selected power supply output is switched onto the output path. Since the present invention incrementally switches small amounts of power, switching losses are substantially mitigated.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a block diagram of a high frequency amplification system utilizing envelope elimination and restoration.

Fig. 2 is a block diagram of the envelope amplifier of the present invention.

Fig. 3 is a block diagram showing a typical regulator suitable for use in the envelope amplifier of the present invention.

Fig. 4 is a simplified diagramatic representation of the DC to DC converter utilized in the envelope amplifier of the present invention.

Fig. 5 is schematic diagram illustrating a typical power switch suitable for use in connection with the envelope amplifier of the present invention.

Fig. 6 is a schematic diagram of the comparator used in the envelope amplifier of the present invention.

Fig. 7(a) shows a typical input signal of the form S(t).

Fig. 7(b) shows the form of the signal output from the detector utilized in an illustrative envelope elimination and restoration system in response to the input of the signal S(t) of Fig. 7(a).

Fig. 7(c) shows the form of the signal output from an envelope amplifier of an envelope elimination and restoration system in response to the input of the signal of the form shown in Fig. 7(b).

Fig. 7(d) shows the output of the limiter of an envelope elimination and restoration system in response to the input of the signal of the form shown in Fig.7(a).

Fig. 7(e) shows the output of an RF amplifier of an envelope elimination and restoration system in response to the input of the signal of the form shown in Fig. 7(a) when powered by a signal of the form shown in Fig. 7(c).

DESCRIPTION OF THE INVENTION

The present invention provides an envelope amplifier which extends the signal bandwidth over which a linear amplifier employing envelope elimination and restoration can be made to operate efficiently. The invention exhibits lower switching losses than a conventional amplifier using a variable duty cycle converter for envelope amplification.

A typical EER system is shown in Fig. 1. The envelope is removed from the input signal S(t) by a limiter 12. The limiter 12 supplies an amplitude limited phase and/or frequency modulated signal as an input to an RF amplifier 14. The envelope is restored by the combination of a conventional power detector 16 and an envelope amplifier 20. The envelope amplifier 20 amplifies the envelope of the input signal, as detected by the power detector 16, and uses it to modulate the power supply of the RF amplifier 14. By amplifying the phase and envelope components of the input signal separately, a high efficiency RF amplifier operating with constant drive power is achieved. If the envelope amplifier is of sufficiently high efficiency, the overall efficiency of the system may exceed that of a linear Class A or Class B amplifier which would otherwise be required to deal with the variable amplitude signal.

As shown in Fig. 2, the present invention provides a high efficiency envelope amplifier 20 which includes a regulator 22, a DC to DC converter 24, a plurality of switches 26 - 38 (even numbers only), a plurality of diodes 40 - 54 (even numbers only), and a comparator 60. The components of the amplifier 20 are designed and selected for optimum efficiency.

The regulator 22 receives DC input from a battery or an array of solar cells (not shown) and provides a regulated voltage for the DC to DC converter 24. An illustrative implementation of the regulator 22 is shown

in Fig. 3. For optimal efficiency, the series pass stage 62 is supplied with a floating voltage pedestal 64 (e.g. 4 volts) by the DC to DC converter 24. A linear comparator 66 monitors the output of the series pass stage 62 through a voltage divider provided by resistors R1 and R2. The linear comparator 66 compares the sensed output level to a reference level and controls the series pass stage 62 through a buffer stage 68 and a driver stage 70. The output is filtered by a set of capacitors 72. The 'on' command is supplied through a first buffer 74 while the 'off' command is supplied through a second buffer 76. Undervoltage protection is provided by an undervoltage turnoff circuit 78. Those of ordinary skill in the art will recognize additional techniques for providing a regulated supply to the DC to DC converter 24 within the scope of the invention.

A simplified diagramatic representation of the DC to DC converter 24 is shown in Fig. 4. A power supply integrated circuit (PSIC) 80 provides clock drive to a pair of complementary drive stages 82 and 84. The drive stages 82 and 84 drive switching transistors 86 and 88 respectively which in turn drive the primary of a transformer 90. A plurality of rectified filtered DC outputs are provided by pairs of taps from the secondary of the transformer 90, e.g. T11 and T13, diodes 98, and one or more elements of the RC network of capacitors C1 through C9 and resistors R1 through R8. In operation, a starter circuit 92 receives input from the regulator 22 and initiates the operation of the power supply integrated circuit 80 and the drive stages 82 and 84. Power is subsequently supplied to the PSIC 80 and the drive stages 82 and 84 by a rectified DC output (e.g. 13

volts) of the transformer 90. The DC to DC converter 24 thus provides multiple output voltage levels to the switches 26 through 38.

The switches 26 - 38 allow the comparator 60 to select appropriate output levels of the DC to DC converter for switching onto the output bus 56 in response to variations in the detected envelope input voltage. An illustrative implementation of a typical power switch 26 is shown in Fig. 5. For efficiency, the switch is floated about the supply voltage V_{CC1} by taps T9/T15 and T11/T13 at 51 and 53 respectively. These taps are adjacent to the tap T10/T14 which provides the supply voltage V_{CC1} at 55 for the switch 26.

Input from the comparator 60 turns on transistor Q1 which pulls down the voltage at point A turning on transistor Q3. Q3 then activates transistors Q5 and Q6. When Q6 is on, the input voltage from the tap T10 at 55 is passed to the output bus 56. When the input from the comparator 60 is removed, Q1 and Q3 go off, Q2 and Q4 go on, Q6 goes off, and the switch input 55 is isolated from the output bus 56 via a diode e.g. 42.

Fig. 6 shows an illustrative implementation of the comparator 60. The detected envelope is received at the input terminal 99 from the detector 16. A voltage drop is developed across a resistor R13 which supplies the input to a plurality of operational amplifiers 100 - 112. The operational amplifiers act as comparators. The reference inputs are provided by a voltage divider network of resistors R14 - R21, which are connected between a reference voltage (+) and ground. Thus, for example, op amp 100 compares the envelope input at its (+) terminal with the reference voltage at the junction of the resistors R14 and R15. With the exception of the first op amp 100, each op amp provides complementary outputs O and O' to two of the AND gates 116 - 128. This allows each op amp to turn off the output gate of the

preceding op amp whenever it is activated. For example, since op amp 100 has a single output, AND gate 116 will be on whenever the first op amp 100 is on and the second op amp 102 is off. When the envelope input voltage increases above the threshold of the second op amp 102, the second op amp 102 is activated, its O output goes high and its O' output goes low. This turns off AND gate 116 and turns on AND gate 118. Thus, the AND gates 116 - 128 selectively activate switches 26 - 38 respectively, depending on the amplitude of the input signal.

In operation, and in reference to Fig. I, when an input signal S(t) of the form shown in Fig. 7(a) is received by the detector at point 'a', the detector 16 outputs at signal at point 'b' of the form shown in Fig. 7(b). The envelope amplifier 20 of the present invention outputs an amplified quantized replica of the input envelope at point 'c' of the form shown in Fig. 7(c). This signal provides the current capability, hence the power capability, to power the RF amplifier 14 to efficiently replicate the envelope of the input signal. The signal input to the RF amplifier 14 at point 'd' is the phase and frequency information of the input signal S(t). The envelope has been removed from this signal by the limiter 12 so that the signal has the form shown in Fig. 7(d). The RF amplifier 14 provides the system output at point 'e' of the form shown in Fig. 7(e). Switching losses are mitigated in the present invention by the switching of relatively small amounts of power.

While the high efficiency envelope amplifier of the present invention has been described with reference to an illustrative embodiment for a particular application, it is understood that the invention is not limited thereto.

Those of ordinary skill in the art and access to the teachings provided above will recognize additional modifications, applications, and embodiments within the scope thereof. For example, the invention is not limited to a particular implementation of the power supply, the power switches, or the comparator. While the present invention provides an power efficient envelope amplifier of particular utility in high efficiency amplifiers using the EER technique, the invention is not limited thereto. The invention may be used in any system where it is desired to provide a quantized replica of an input signal.

It is therefore intended by the appended Claims to cover any and all such modifications, applications and embodiments. Thus,

CLAIMS

WHAT IS CLAIMED IS:

1. An envelope amplifier having an output bus and comprising:

power supply means for providing plural output levels;

comparator means for comparing the amplitude of an input signal to one of several threshold levels; and

switch means operated by said comparator means to select output levels from said power supply for connection to the output bus of said envelope amplifier.

2. The envelope amplifier of Claim 1 wherein said power supply means includes a DC to DC converter.

3. The envelope amplifier of Claim 2 wherein said power supply means includes voltage regulator means for supplying power to said DC to DC converter.

4. The envelope amplifier of Claim 1 including diode logic between the switch means and the output path.

5. A high frequency amplifier for an input signal having variable amplitude including:

limiter means for removing the amplitude variations from said input signal;

detector means for detecting the amplitude variations of said input signal;

envelope amplification means for amplifying said detected amplitude variations, said envelope amplification means including power supply means for providing plural output levels; comparator means for comparing the amplitude of an input signal to one of several threshold levels; and switch means operated by said comparator means to select output levels from said power supply for connection to the output bus of said envelope amplifier; and

means for combining the output of said limiter means with the output of said envelope amplification means.

6. The high frequency amplifier of Claim 5 wherein said power supply means includes a DC to DC converter.

7. The high frequency amplifier of Claim 5 wherein said means for combining the output of said limiter means with the output of said envelope amplification means is an amplifier.

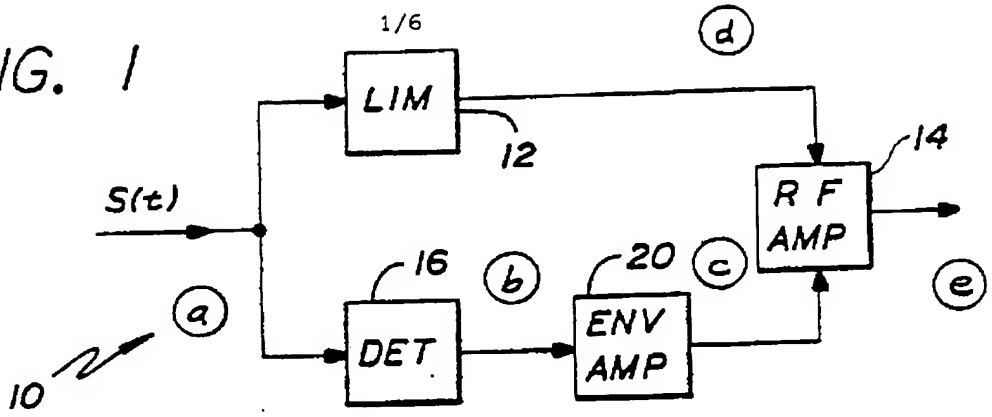
8. A method for provided a quantized replica of an amplitude varying input signal including the steps of:

a) providing a multiplicity of power outputs;

b) comparing the instantaneous amplitude of the input signal to plural predetermined thresholds and

c) selectively switching said power outputs onto an output bus in response to the comparison of the input signal to said predetermined thresholds.

FIG. 1


LIM
12
d
14
R F AMP
S(t)
16
b
20
c
e
a
DET
ENV AMP
10

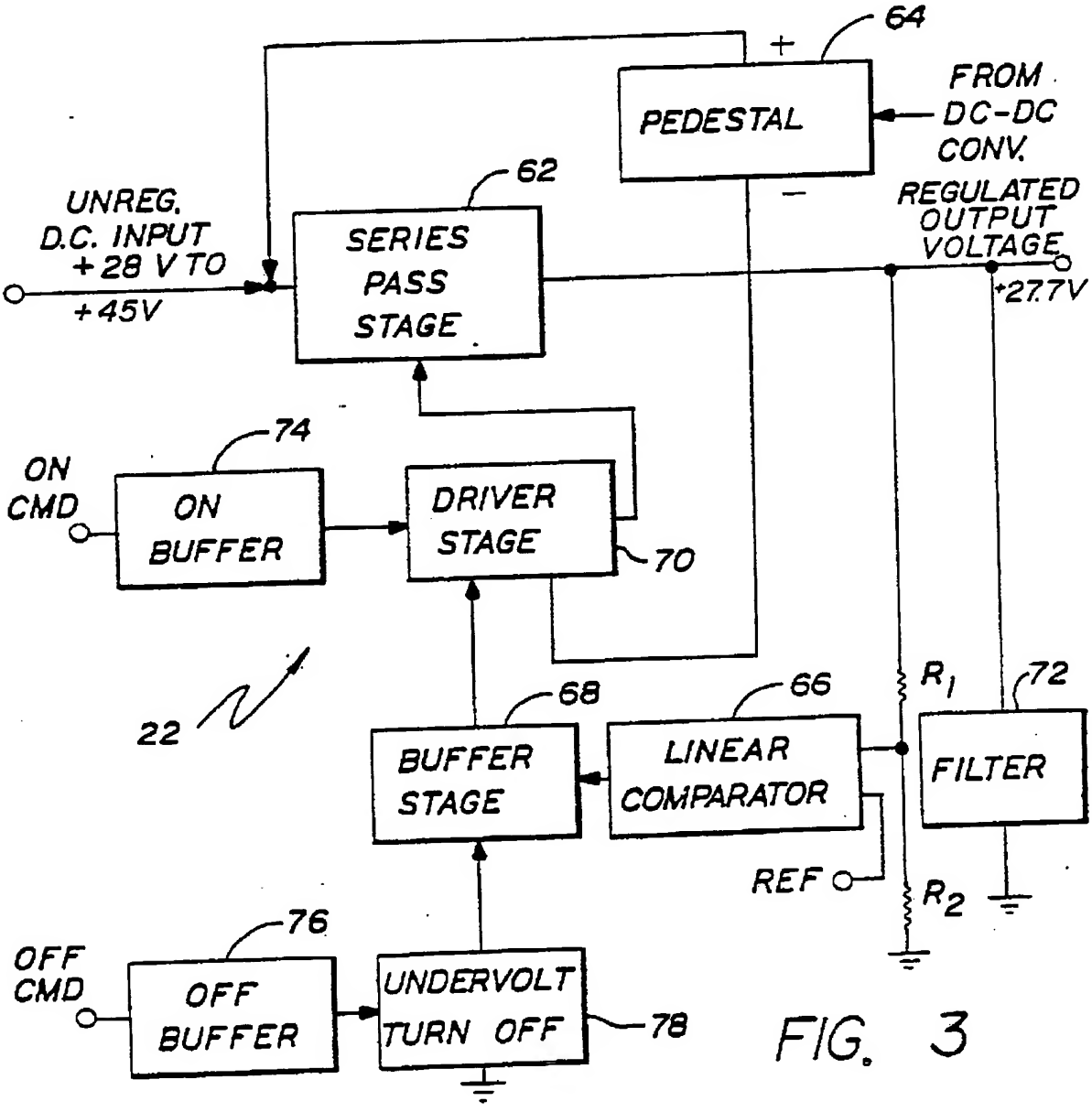
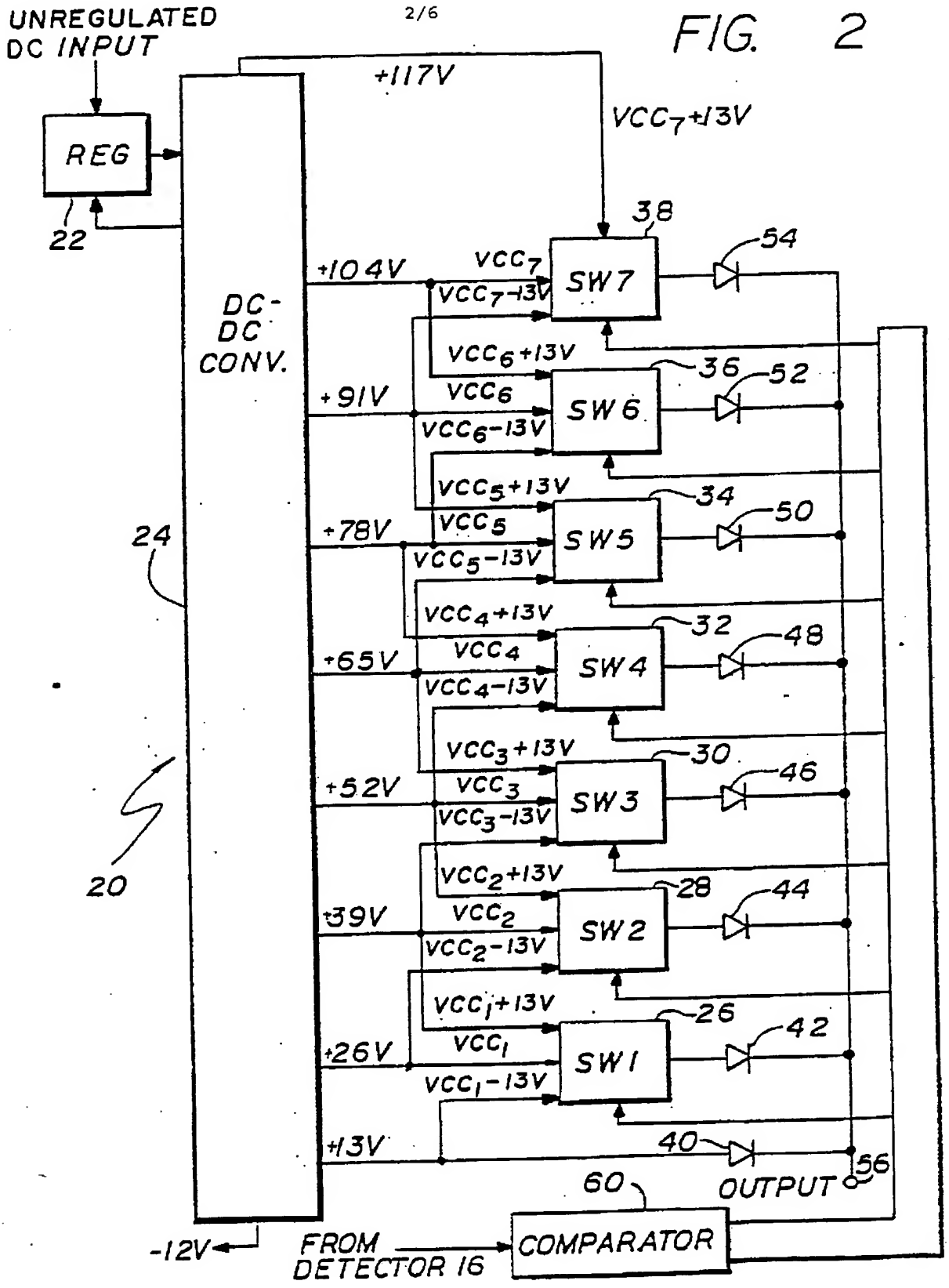

64
+
PEDESTAL
FROM DC-DC CONV.
62
UNREG. D.C. INPUT +28 V TO +45V
SERIES PASS STAGE
REGULATED OUTPUT VOLTAGE
+27.7V
74
ON CMD
ON BUFFER
DRIVER STAGE
70
22
68
66
R_1
72
BUFFER STAGE
LINEAR COMPARATOR
FILTER
REF
R_2
76
OFF CMD
OFF BUFFER
UNDERVOLT TURN OFF
78

FIG. 3

FIG. 2


UNREGULATED DC INPUT
REG
22
+117V
VCC7+13V
DC-DC CONV.
24
20
38
54
+104V
VCC7
VCC7-13V
SW7
VCC6+13V
36
52
+91V
VCC6
VCC6-13V
SW6
VCC5+13V
34
50
+78V
VCC5
VCC5-13V
SW5
VCC4+13V
32
48
+65V
VCC4
VCC4-13V
SW4
VCC3+13V
30
46
+52V
VCC3
VCC3-13V
SW3
VCC2+13V
28
44
+39V
VCC2
VCC2-13V
SW2
VCC1+13V
26
42
+26V
VCC1
VCC1-13V
SW1
+13V
40
56
OUTPUT
60
COMPARATOR
-12V
FROM DETECTOR 16

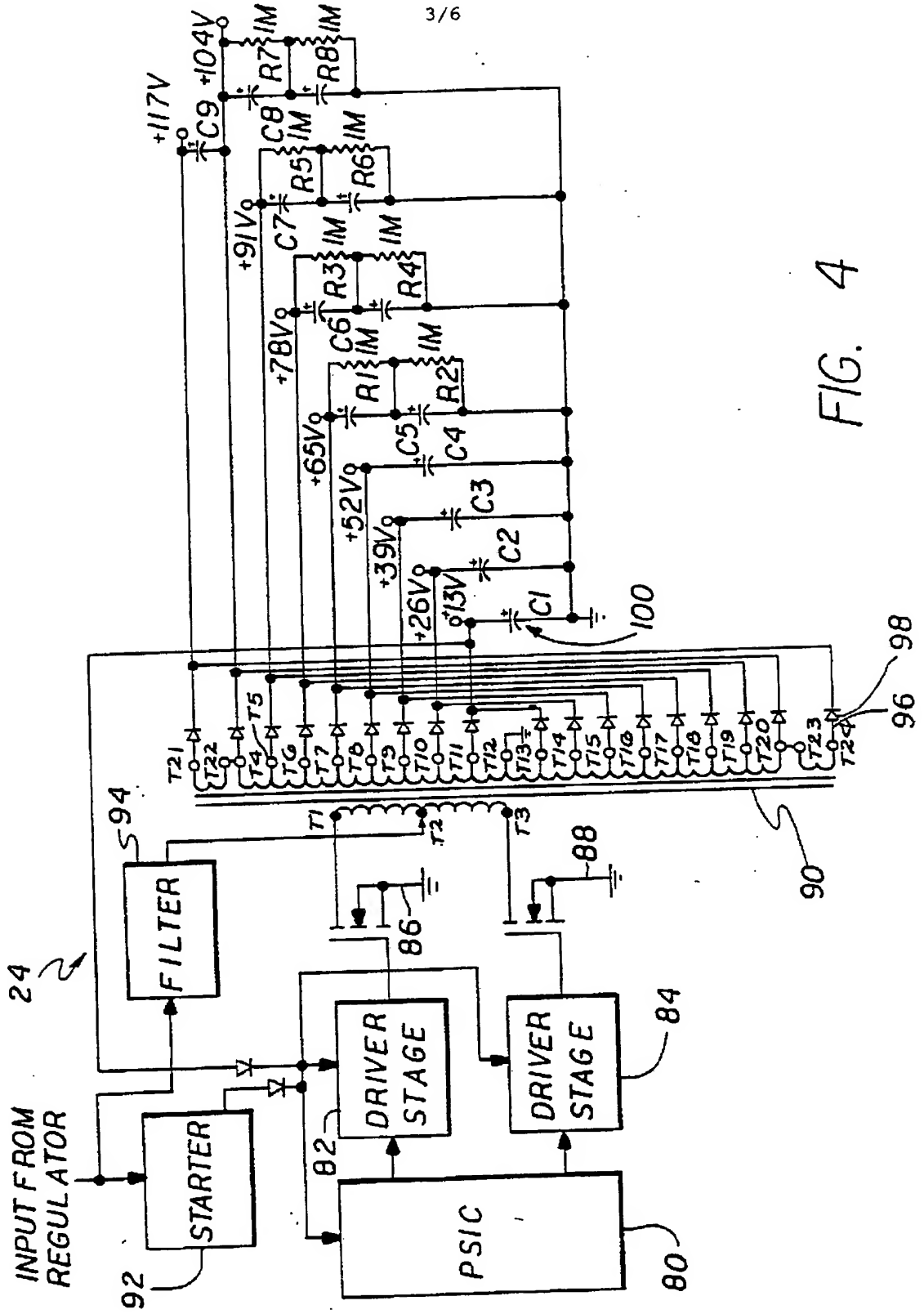
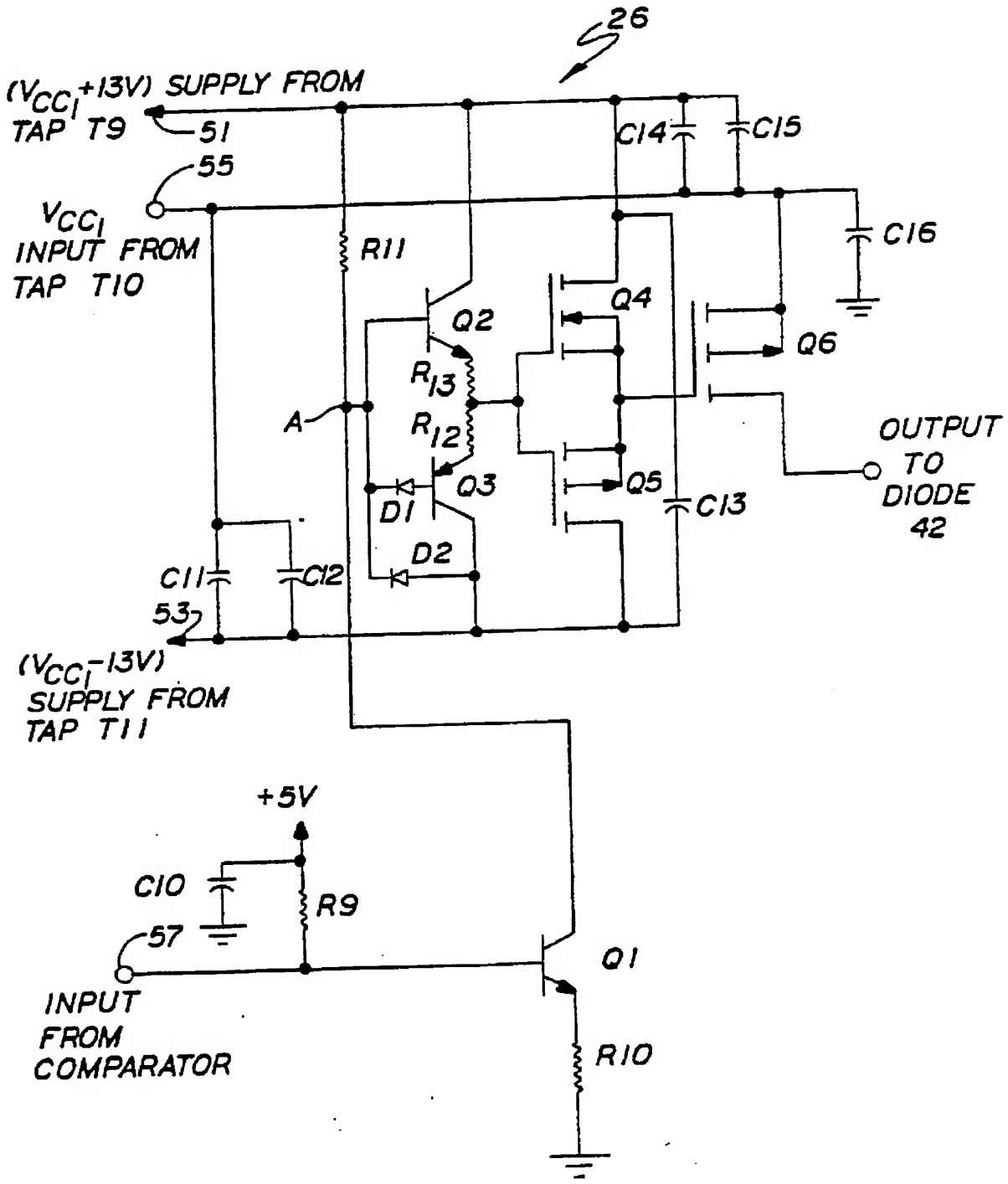

+117V
+104V
+91V
+78V
+65V
+52V
+39V
+26V
+13V
C9
C8
C7
C6
C5
C4
C3
C2
C1
R7
R8
R5
R6
R3
R4
R1
R2
IM
100
98
96
90
94
88
86
24
FILTER
DRIVER STAGE
DRIVER STAGE
84
82
INPUT FROM REGULATOR
STARTER
92
PSIC
80
T1
T2
T3
T4
T5
T6
T7
T8
T9
T10
T11
T12
T13
T14
T15
T16
T17
T18
T19
T20
T21
T22
T23
T24

FIG. 4

FIG. 5


26
(V_{CC_1}+13V) SUPPLY FROM TAP T9
51
55
V_{CC_1} INPUT FROM TAP T10
R11
C14
C15
C16
Q2
Q4
Q6
R_{13}
R_{12}
A
Q3
Q5
D1
D2
C13
OUTPUT TO DIODE 42
C11
C12
53
(V_{CC_1}-13V) SUPPLY FROM TAP T11
+5V
C10
R9
57
INPUT FROM COMPARATOR
Q1
R10

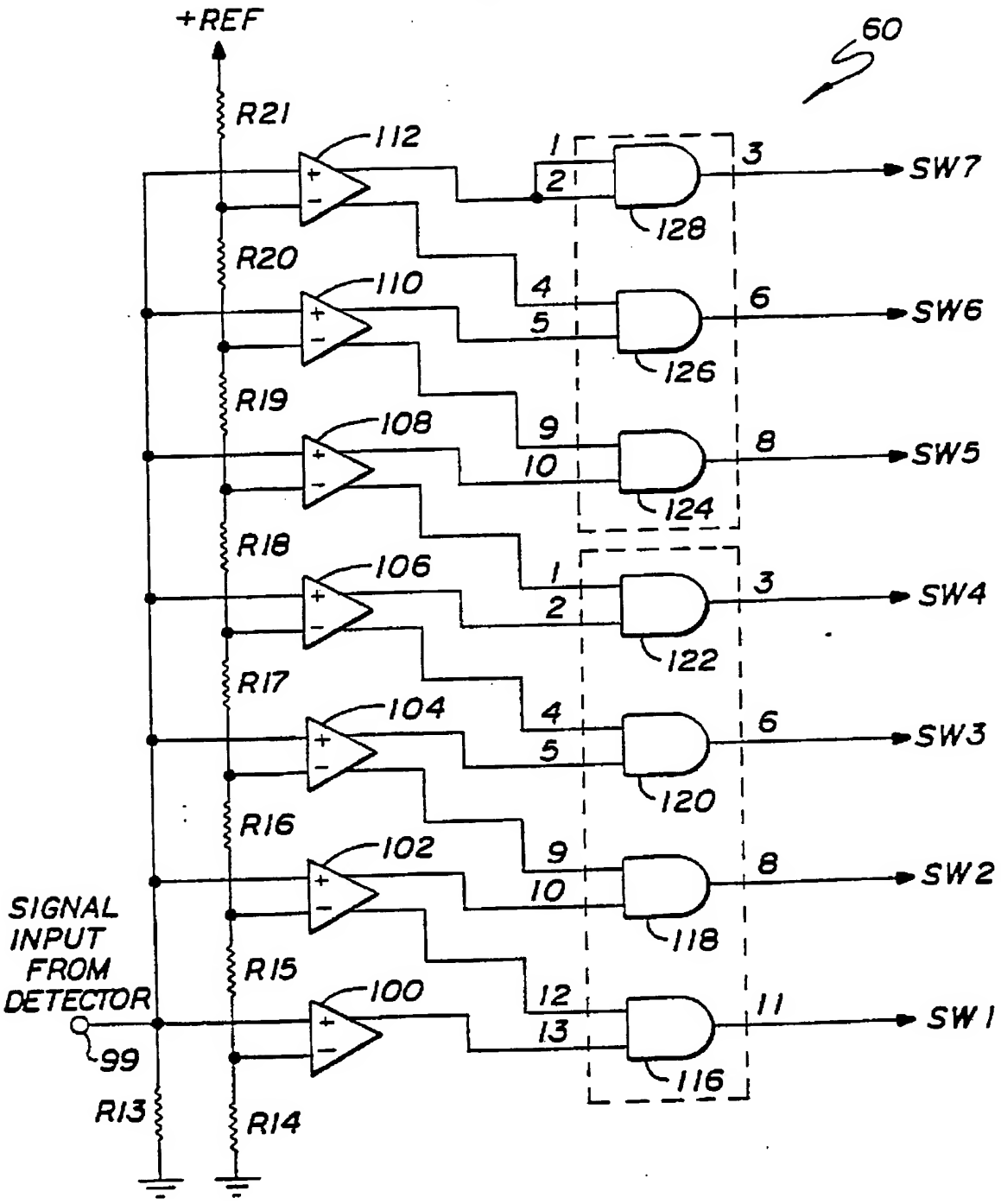

+REF
60
R21
112
1
2
3
SW7
128
R20
110
4
5
6
SW6
126
R19
108
9
10
8
SW5
124
R18
106
1
2
3
SW4
122
R17
104
4
5
6
SW3
120
R16
102
9
10
8
SW2
118
SIGNAL INPUT FROM DETECTOR
R15
100
12
13
11
SW1
99
116
R13
R14

FIG. 6

FIG. 7(a)

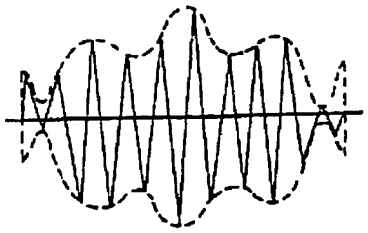


FIG. 7(b)

FIG. 7(d)

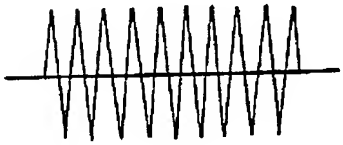


FIG. 7(c)

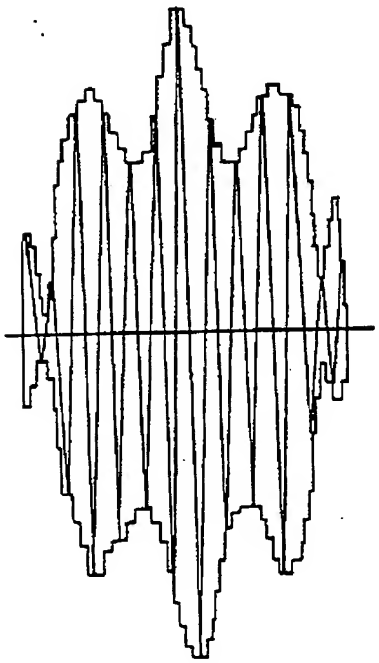


FIG. 7(e)

INTERNATIONAL SEARCH REPORT

International Application No PCT/US 88/01463

I. CLASSIFICATION OF SUBJECT MATTER (if several classification symbols apply, indicate all) [6]

According to International Patent Classification (IPC) or to both National Classification and IPC

IPC[4]: H 03 F 1/02; H 03 F 3/217

II. FIELDS SEARCHED

Minimum Documentation Searched [7]

Classification System	Classification Symbols
IPC[4]	H 03 F

Documentation Searched other than Minimum Documentation to the Extent that such Documents are Included in the Fields Searched [8]

III. DOCUMENTS CONSIDERED TO BE RELEVANT [9]

Category *	Citation of Document, [11] with indication, where appropriate, of the relevant passages [12]	Relevant to Claim No. [13]
X	Patent Abstracts of Japan, volume 6, no. 60 (E-102)(938), 17 April 1982, & JP, A, 572107 (PIONEER K.K.) 7 January 1982	1,4,8
Y	--	5,7
Y	EP, A, 0083727 (HARRIS CORP.) 20 July 1983 see figures 7-9; abstract; page 33, line 17 - page 35, line 3	5,7
A	-- Patent Abstracts of Japan, volume 6, no. 99 (E-111)(977), 8 June 1982, & JP, A, 5732104 (HITACHI SEISAKUSHO K.K.) 20 February 1982	2,3,6
A	-- EP, A, 0151345 (CONTROL CONCEPTS CORP.) 14 August 1985 see figure; page 1, lines 5-10	1,7,8

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"&" document member of the same patent family

IV. CERTIFICATION

Date of the Actual Completion of the International Search	Date of Mailing of this International Search Report
19th August 1988	16 SEP 1988
International Searching Authority: EUROPEAN PATENT OFFICE	Signature of Authorized Officer: P.C.G. VAN DER PUTTEN

ANNEX TO THE INTERNATIONAL SEARCH REPORT ON INTERNATIONAL PATENT APPLICATION NO. US 8801463 SA 22357

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Patent document cited in search report	Publication date	Patent family member(s)	Publication date
EP-A- 0083727	20-07-83	CA-A- 1196396	05-11-85
		US-A- 4580111	01-04-86
EP-A- 0151345	14-08-85	JP-A- 60204265	15-10-85
		US-A- 4628438	09-12-86